

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

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10-12-99
R. Stokes

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Applicant : Rong-Fuh Shyu
Application No. : To Be Assigned
Filed : Herewith
Title : LEAD FRAME FOR A SEMICONDUCTOR CHIP PACKAGE,
SEMICONDUCTOR CHIP PACKAGE INCORPORATING MULTIPLE
INTEGRATED CIRCUIT CHIPS, AND METHOD OF FABRICATING
A SEMICONDUCTOR CHIP PACKAGE WITH MULTIPLE
INTEGRATED CIRCUIT CHIPS

Grp./Div. : To Be Determined
Examiner : To Be Determined

Docket No. : 35761/DBP/S295

1c678 U.S. PTO
09/383150
08/28/99

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Post Office Box 7068
Pasadena, CA 91109-7068
August 24, 1999

Commissioner:

In compliance with the duty of disclosure under 37 CFR §§ 1.56, 1.97 and 1.98, and in accordance with the provisions in the Manual of Patent Examining Procedure §§ 609 and 707.05(b), enclosed is FORM PTO-1449 listing the references that are known to applicant. Copies of each of the listed references are enclosed.

It is respectfully requested that the listed references be considered in the examination of this application and identified on the list of references cited on the patent issuing for this application. Applicant also requests that an initialed copy of FORM PTO-1449 be entered in the application file and returned to applicant with the next communication from the Office in accordance with MPEP § 609.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By D. Bruce Prout
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626/795-9900

DBP/sfc
Enclosures: PTO-1449, w/references

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